BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

IT IS CLAIMED:

1. A method of forming a non-volatile memory integrated circuit, comprising:

growing a layer of dielectric across a surface of the substrate,

depositing a layer of conductive material across the dielectric layer,

removing a portion of the conductive material layer to form a plurality of slots, which leave conductive material layer strips, elongated in a first direction and spaced apart in a second direction, the first and second directions being orthogonal to each other,

thereafter depositing field dielectric over and extending into the plurality of slots between the conductive material layer strips, and

separating the first conductive material layer strips into individual floating gates, thereby forming an array of rows and columns of the floating gates that are individually separated from the substrate surface by the grown layer of dielectric sandwiched therebetween.

2. The method of claim 1, additionally comprising forming conductive ion strips in the substrate surface that are elongated in the second direction continuously across a plurality of rows of floating gates and regularly spaced apart in the first direction in between columns of floating gates.

3. The method of claim 2, additionally comprising forming trenches elongated in the first direction across a plurality of ion implant regions and spaced apart in the second direction with positions in between the rows of floating gates, and filing the trenches with a dielectric material, the trenches being shallow enough so as not to interrupt the conductivity of the substrate ion strips along their lengths.

4. The method of claim 3, additionally comprising providing peripheral circuits adjacent the array of floating gates, forming at least one trench between the array and the peripheral circuits and filing said at least one trench with a dielectric material, thereby to electrically isolate the array and peripheral circuits, said at

least one trench being significantly deeper than the trenches between the rows of floating gates.

5. The method of claim 1, additionally comprising providing peripheral circuits adjacent the array of floating gates, forming at least one trench between the array and the peripheral circuits and filing said at least one trench with a dielectric material, thereby to electrically isolate the array and peripheral circuits.

6. The method of claim 1, wherein depositing the conductive layer includes depositing polysilicon material.

7. A method of forming a non-volatile memory array on a substrate, comprising:

growing a layer of dielectric across a surface of the substrate,

depositing a first layer of polysilicon across the dielectric layer,

removing a portion of the first polysilicon layer to form a first plurality of slots, which leave first polysilicon layer strips, elongated in a first direction and spaced apart in a second direction, the first and second directions being orthogonal to each other,

thereafter depositing field dielectric over and extending into the first plurality of slots between the first polysilicon layer strips,

removing a top portion of the field dielectric to form a uniform surface across the first polysilicon layer strips, thereby leaving field dielectric between the first polysilicon layer strips in the second direction,

thereafter removing a portion of the first polysilicon layer strips and field dielectric in a pattern forming a second plurality of slots continuously elongated in the second direction across a plurality of the first polysilicon layer strips and regularly spaced apart in the first direction, thereby separating the first polysilicon layer strips into segments between the second plurality of slots that have equal lengths in the first direction,

implanting ions into the substrate through the second plurality of slots while the remaining first polysilicon layer strip segments and field oxide act as a mask to block ions from reaching the substrate outside of the second plurality of slots, thereby

forming continuous ion strips implanted into the substrate and elongated in the second direction across a plurality of the first polysilicon layer strips,

thereafter forming, from a second layer of polysilicon deposited over said uniform surface and into the second plurality of slots, steering gates elongated in the second direction and spaced apart in the first direction,

separating the individual first polysilicon layer strip segments into two floating gates by removing a portion of the first polysilicon layer strip segments exposed between adjacent steering gates, thereby to form spaces between adjacent floating gates, and

thereafter forming, from a third layer of polysilicon deposited over the steering gates and into the spaces between adjacent floating gates, word lines spaced apart in the second direction and elongated across individual rows of floating gates in the first direction.

8. The method of claim 7, wherein the step of forming steering gates includes using an etch mask over the deposited second polysilicon layer without self-alignment with the second plurality of slots of the first polysilicon layer.

9. The method of claim 7, wherein the step of forming steering gates includes orienting the steering gates with spaces between them being self-aligned in the first direction intermediate of adjacent ones of the second plurality of slots in the first polysilicon layer.

10. The method of claim 7, wherein removing the first polysilicon layer strips and field oxide in a pattern forming a second plurality of slots includes:

forming first elements of a dielectric mask with lengths oriented in the second direction across the first polysilicon layer strips and field oxide in between and being regularly spaced apart in the first direction, and

forming dielectric spacers as second elements of the dielectric mask along both sides of the first elements, reducing the width of said second plurality of slots through which the ions are implanted.

11. The method of claim 10, wherein forming the steering gates includes:

after implanting the ions into the substrate, removing the spacers of the dielectric mask while leaving the mask first elements in place,

depositing the second layer of polysilicon over and between the mask first elements,

removing any portion of the second layer of polysilicon that is above the mask first elements, and

thereafter removing the mask first elements, whereby spaces between the steering gates in the first direction are formed.

12. The method of claim 11, wherein separating the individual first polysilicon layer strip segments includes etching the first polysilicon layer strip segments through the spaces between the steering gates.

13. The method of claim 12, wherein forming word lines includes depositing the third layer of polysilicon into the spaces between adjacent floating gates through the spaces between the steering gates.

14. The method of claim 7, wherein removing the top portion of the field dielectric includes using chemical-mechanical-planarization (CMP).

15. The method of claim 7, which additionally comprises, after separating the individual first polysilicon layer strip segments into two floating gates, depositing a dielectric material into the spaces formed between adjacent floating gates in a manner to fill a portion of those spaces, the subsequent step of forming word lines including depositing the third layer of polysilicon into the spaces over the deposited dielectric material.

16. The method of claim 7, which additionally comprises, after separating the individual first polysilicon layer strip segments into two floating gates, forming recesses in the substrate that are aligned with the spaces between adjacent

floating gates, and wherein the subsequent step of forming word lines includes depositing the third layer of polysilicon though the spaces between adjacent floating gates and into the substrate recesses.

17. The method of claim 16, wherein separating the first polysilicon layer strip segments into two floating gates additionally includes forming spacers on side walls of the adjacent steering gates in order to reduce the extent of the first polysilicon layer strip segments that are exposed between adjacent steering gates.

18. The method of claim 7, which additionally comprises, prior to forming the steering gates, reducing a thickness of the field dielectric between the first polysilicon layer strips to a level below a top surface and a top portion of the sides of the first polysilicon layer strips, and wherein the subsequent formation of the steering gates includes wrapping the steering gates around the top surface and side portion of the sides of the first polysilicon layer strips.

19. The method of claim 7, which additionally comprises, prior to implanting ions into the substrate through the second plurality of slots, narrowing a width of the second plurality of slots in the first direction by forming spacers along sides of the second plurality of slots, thereby to subsequently implant ions through the second plurality of slots after being narrowed.

20. The method of claim 19, which additionally comprises, after implanting ions into the substrate through the narrowed second plurality of slots, removing the spacers.

21. The method of claim 7, which additionally comprises, prior to forming the second plurality of slots, depositing a further layer of polysilicon over the uniform surface and separating the further layer into further strips positioned on top of the first polysilicon layer strips, the further strips being elongated in a first direction and spaced apart in the second direction by a distance that is less than the distance between the first polysilicon layer strips in the second direction, the further strips becoming part of

the first polysilicon strips during subsequent processing that forms the second plurality of slots and separates the first polysilicon layer strip segments.

22. A method of forming a non-volatile memory array on a substrate, comprising:

growing a layer of dielectric across a surface of the substrate,

depositing a first layer of polysilicon across the dielectric layer,

removing a portion of the first polysilicon layer to form a first plurality of slots, which leave first polysilicon layer strips, elongated in a first direction and spaced apart in a second direction, the first and second directions being orthogonal to each other,

thereafter depositing field dielectric over and extending into the first plurality of slots between the first polysilicon layer strips,

removing a top portion of the field dielectric to form a uniform surface across the first polysilicon layer strips, thereby leaving field dielectric between the first polysilicon layer strips in the second direction,

thereafter removing a portion of the first polysilicon layer strips and field dielectric in a pattern forming a second plurality of slots continuously elongated in the second direction across a plurality of the first polysilicon layer strips and regularly spaced apart in the first direction, thereby separating the first polysilicon layer strips into individual floating gates,

implanting ions into the substrate through alternate ones of the second plurality of slots, thereby forming continuous ion strips implanted into the substrate and elongated in the second direction across a plurality of rows of floating gates,

thereafter forming polysilicon elements within the individual second plurality of slots at least between adjacent floating gates,

forming, from another layer of polysilicon deposited over said uniform surface and in contact with the polysilicon elements within said alternate ones of the second plurality of slots, steering gates elongated in the second direction and spaced apart in the first direction, and

forming, from a further layer of polysilicon deposited over the steering gates and in contact with the polysilicon elements within others of the second plurality of

slots than said alternate ones, word lines spaced apart in the second direction and elongated across individual rows of floating gates in the first direction.

23. A non-volatile memory formed on an integrated circuit substrate, comprising:

an array of memory cells formed in a first region of the substrate,

circuits peripheral to the memory cell array including decoders, drivers and sense amplifiers that are formed in a second region of the substrate that does not overlap the first region, and

a trench formed in the substrate between the first and second regions, the trench being at least 3000 Angstroms in depth and filled with a dielectric material, thereby to isolate the memory cell array and peripheral circuits.